1   **Claims**

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3   We claim the following invention:

4   1.   A System-on-Chip (SOC) apparatus having a latency-tolerant architecture,

5   comprising:

6   a processor core;

7   one or more peripherals; and

8   a first internal bus that couples said processor core to said peripheral(s) and carries

9   signals from signal initiators to signal targets, said first internal bus has a latency tolerant

10   signal protocol that allows an arbitrary number of pipeline stages between any signal

11   initiator and any signal target.

12   2.   The System-on-Chip (SOC) apparatus of claim 1 wherein said one or more

13   peripherals further comprises one or more DMA-type peripherals, and said apparatus

14   further comprises:

15   a memory subsystem; and

16   a second internal bus that couples said processor core to said memory subsystem

17   and to said DMA-type peripherals, said second internal bus carries signals from signal

18   initiators to signal targets, said second internal bus has a latency tolerant signal protocol

19   that allows an arbitrary number of pipeline stages between any signal initiator and any

20   signal target.

21   3.   The System-on-Chip (SOC) apparatus of claim 1 or claim 2, wherein said signals

22   are point-to-point and registered signals, and said latency tolerant signal protocol further

23   comprises full handshaking.

1   4.   The System-on-Chip (SOC) apparatus of claim 1 or claim 2, wherein said pipeline

2   stages further comprise one or more of the following: flip-flop, multiplexing router, or

3   decoding router.

4   5.   The System-on-Chip (SOC) apparatus of claim 2, wherein said first internal bus and

5   said second internal bus have overlapping topologies, each topology further comprising

6   one or more of the following topologies: matrix fabric (or woven) topology, point-to-point

7   topology, bridged topology, or bussed topology.

8   6.   A System-on-Chip (SOC) system having a latency-tolerant architecture, comprising:

9   a processor core;

10   one or more peripherals; and

11   a first internal bus that couples said processor core to said peripheral(s) and carries

12 signals from signal initiators to signal targets, said first internal bus has a latency tolerant

13 signal protocol that allows an arbitrary number of pipeline stages between any signal

14 initiator and any signal target.

15 7.   The System-on-Chip (SOC) system of claim 6 wherein said one or more

16 peripherals further comprises one or more DMA-type peripherals, and said system further

17 comprises:

18   a memory subsystem; and

19   a second internal bus that couples said processor core to said memory subsystem

20 and to said DMA-type peripherals, said second internal bus carries signals from signal

21 initiators to signal targets, said second internal bus has a latency tolerant signal protocol

22 that allows an arbitrary number of pipeline stages between any signal initiator and any

1   signal target.

2   8.   The System-on-Chip (SOC) system of claim 6 or claim 7, wherein said signals are

3   point-to-point and registered signals, and said latency tolerant signal protocol further

4   comprises full handshaking.

5   9.   The System-on-Chip (SOC) system of claim 6 or claim 7, wherein said pipeline

6   stages further comprise one or more of the following: flip-flop, multiplexing router, or

7   decoding router.

8   10.   The System-on-Chip (SOC) system of claim 7, wherein said first internal bus and

9   said second internal bus have overlapping topologies, each topology further comprising

10   one or more of the following topologies: matrix fabric (or woven) topology, point-to-point

11   topology, bridged topology, or bussed topology.

12   11.   A method to manufacture a System-on-Chip (SOC) apparatus having a latency-

13   tolerant architecture, comprising:

14   providing a processor core;

15   providing one or more peripherals; and

16   coupling a first internal bus to said processor core and to said peripheral(s), said

17   first internal bus carries signals from signal initiators to signal targets, said first internal bus

18   has a latency tolerant signal protocol that allows an arbitrary number of pipeline stages

19   between any signal initiator and any signal target.

20   12.   The method of claim 11 wherein said one or more peripherals further comprises

21   one or more DMA-type peripherals, and said method further comprises:

22   providing a memory subsystem; and

1   coupling a second internal bus to said processor core, to said memory subsystem,

2 and to said DMA-type peripherals, said second internal bus carries signals from signal

3 initiators to signal targets, said second internal bus has a latency tolerant signal protocol

4 that allows an arbitrary number of pipeline stages between any signal initiator and any

5 signal target.

6 13. The method of claim 11 or claim 12, wherein said signals are point-to-point and

7 registered signals, and said latency tolerant signal protocol further comprises full

8 handshaking.

9 14. The method of claim 11 or claim 12, wherein said pipeline stages further comprise

10 one or more of the following: flip-flop, multiplexing router, or decoding router.

11 15. The method of claim 12, wherein said first internal bus and said second internal bus

12 have overlapping topologies, each topology further comprising one or more of the following

13 topologies: matrix fabric (or woven) topology, point-to-point topology, bridged topology, or

14 bussed topology.

15 16. A method of using a System-on-Chip (SOC) apparatus having a latency-tolerant

16 architecture, comprising:

17   providing a processor core;

18   providing one or more peripherals; and

19   carrying signals from signal initiators to signal targets over a first internal bus that

20 couples said processor core to said peripheral(s), said first internal bus has a latency

21 tolerant signal protocol that allows an arbitrary number of pipeline stages between any

22 signal initiator and any signal target.

1 17.   The method of claim 16 wherein said one or more peripherals further comprises

2 one or more DMA-type peripherals, and said method further comprises:

3   providing a memory subsystem; and

4   carrying signals from signal initiators to signal targets over a second internal bus

5 that couples said processor core to said memory subsystem and to said DMA-type

6 peripherals, said second internal bus has a latency tolerant signal protocol that allows an

7 arbitrary number of pipeline stages between any signal initiator and any signal target.

8 18.   The method of claim 16 or claim 17, wherein said signals are point-to-point and

9 registered signals, and said latency tolerant signal protocol further comprises full

10 handshaking.

11 19.   The method of claim 16 or claim 17, wherein said pipeline stages further comprise

12 one or more of the following: flip-flop, multiplexing router, or decoding router.

13 20.   The method of claim 17, wherein said first internal bus and said second internal bus

14 have overlapping topologies, each topology further comprising one or more of the following

15 topologies: matrix fabric (or woven) topology, point-to-point topology, bridged topology, or

16 bussed topology.